WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate comprising a silicon germanium (SiGe) layer formed on a base layer;

a plurality of field effect transistors (FET) including at least one first FET and at least one second FET formed on the semiconductor substrate; wherein

said first FET comprises a gate electrode formed over the SiGe layer, and a gate oxide layer interposed between the gate electrode and the SiGe layer, wherein the gate oxide layer is formed immediately adjacent to and in contact with the SiGe layer; and

said second FET comprises a silicon layer formed on the SiGe layer, a gate oxide layer formed on the silicon layer, and a gate electrode formed on the gate oxide layer.

2. The semiconductor device of claim 1, wherein said base layer comprises silicon.

3. The semiconductor device of claim 1, wherein the silicon layer comprises strained silicon.

4. The semiconductor device of claim 1, further comprising isolation regions interposed between the first FET and second FET.

5. The semiconductor device of claim 4, wherein the isolation regions are shallow trench isolation regions.

6. The semiconductor device of claim 1, wherein the silicon layer has a thickness of about 50 Å to about 500 Å.

7. The semiconductor device of claim 1, wherein the SiGe layer comprises a first sublayer, said first sublayer has a composition that is graded from about 0% Ge at the SiGe layer/substrate interface up to about 30% Ge.

8. The semiconductor device of claim 1, wherein said gate oxide layer comprises a high-k dielectric.

9. The semiconductor device of claim 1, wherein the gate oxide layer has a thickness of about 10 Å to about 50 Å.

10. A method of manufacturing semiconductor devices, the method comprising:

providing a semiconductor substrate comprising a SiGe layer formed on a base layer, and a silicon layer formed on the SiGe layer, wherein the semiconductor substrate comprises first regions and second regions spaced apart from each other by interposed isolation regions;

selectively removing at least a portion of the silicon layer only in the first region;

implanting dopant in the first and second regions;

forming a gate oxide layer in the first and second regions; and

forming a gate electrode layer over the gate oxide layer.

11. The method according to clam 10, wherein a p-type dopant is implanted in the first region and an n-type dopant is implanted in the second region.

12. The method according to claim 10, wherein substantially all of the silicon layer is removed from the first region.

13. The method according to claim 10, further comprising forming a high-k dielectric layer on the SiGe layer of the first region after removing substantially all of the silicon layer.

14. The method according to claim 13, wherein the high-k dielectric layer comprises dielectric selected from the group consisting of zirconium oxide or hafnium oxide.

15. The method according to claim 10, further comprising oxidizing the silicon layer to form the gate oxide.

16. The method according to claim 15, wherein substantially all of the remaining silicon layer in the first region is oxidized to form the gate oxide layer.

17. The method according to claim 10, wherein the silicon layer is formed to a thickness of about 50 Å to about 500 Å.

18. The method according to claim 10, wherein the gate oxide layer has a thickness of about 10 Å to about 50 Å.

19. The method according to claim 10, wherein the silicon layer comprises strained silicon.

20. The method according to claim 10, wherein the SiGe layer comprises a first sublayer and said first sublayer has a composition that is graded from about 0% Ge at the SiGe layer/base layer interface up to about 30% Ge.